What is claimed is:

1. A one time programmable solid-state device comprising:

a programmable memory unit embedded in a die within the one time programmable solid-state device;

a driver circuit that programs the programmable memory unit; and

an access circuit that enables access to the programmable memory unit.

2. The one time programmable solid-state device of claim 1 wherein the programmable memory unit includes a number of memory cells with each memory cell of the number of memory cells having a gate.

3. The one time programmable solid-state device of claim 2 wherein the memory cells are arranged in a two-dimensional array having a number of rows of memory cells and a number of columns of memory cells.

4. The one time programmable solid-state device of claim 3 wherein the number of rows of memory cells is equal to a predetermined number, and the number columns of memory cells is equal to the predetermined number.

5. The one time programmable solid-state device of claim 2 wherein each memory cell in the number of memory cells is a capacitor.

6. The one time programmable solid-state device of claim 2 wherein each memory cell in the number of memory cells is a transistor.

7. The one time programmable solid-state device of claim 6 wherein the transistor is a field-effect transistor (FET).

8. The one time programmable solid-state device of claim 2 wherein a programming a code is stored in the programmable memory unit.

9. The one time programmable solid-state device of claim 8 wherein the code is a serial number.

10. The one time programmable solid-state device of claim 8 wherein the code is a product identifier.

11. The one time programmable solid-state device of claim 2 wherein the solid-state device is an application specific integrated circuit (ASIC) having at least one predetermined configuration value in the programmable memory unit.

12. The one time programmable solid-state device of claim 2 wherein the number of memory cells contains an address of at least one defective pixel that is located in an imaging device on the die of the one time programmable solid-state device.

13. The one time programmable solid-state device of claim 12 wherein at least one memory cell of the number of memory cells is permanently encoded.

14. The one time programmable solid-state device of claim 13 wherein the at least one memory storage cell is permanently encoded by application of an effective voltage to the gate at least equal to a breakdown voltage of a gate oxide on the surface of the gate.

15. The one time programmable solid-state device of claim 1 wherein the driver circuit and access circuit are embedded in the die.

16. The one time programmable solid-state device of claim 15 wherein the programmable memory unit includes a number of memory cells with each memory cell of the number of memory cells having a gate.

17. The one time programmable solid-state device of claim 16 wherein the memory cells are arranged in a two-dimensional array having a number of rows of memory cells and a number of columns of memory cells.

18. The one time programmable solid-state device of claim 17 wherein the number of rows of memory cells is equal to a predetermined number, and the number columns of memory cells is equal to the predetermined number.

19. The one time programmable solid-state device of claim 16 wherein each memory cell in the number of memory cells is a capacitor.

20. The one time programmable solid-state device of claim 16 wherein each memory cell in the number of memory cells is a transistor.

21. The one time programmable solid-state device of claim 20 wherein the transistor is a field-effect transistor (FET).

22. The one time programmable solid-state device of claim 16 wherein a programming a code is stored in the programmable memory unit.

23. The one time programmable solid-state device of claim 22 wherein the code is a serial number.

24. The one time programmable solid-state device of claim 22 wherein the code is a product identifier.

25. The one time programmable solid-state device of claim 16 wherein the solid-state device is an application specific integrated circuit (ASIC) having at least one predetermined configuration value in the programmable memory unit.

26. The one time programmable solid-state device of claim 16 wherein the number of memory cells contains an address of at least one defective pixel that is located in an imaging device on the die of the one time programmable solid-state device.

27. The one time programmable solid-state device of claim 26 wherein at least one memory cell of the number of memory cells is permanently encoded.

28. The one time programmable solid-state device of claim 27 wherein the at least one memory storage cell is permanently encoded by application of an effective voltage to the gate at least equal to a breakdown voltage of a gate oxide on the surface of the gate.

29. A method for programming a one time programmable solid-state device comprising:

writing, with a driver circuit, to a programmable memory unit embedded in a die within the programmable solid-state device and

accessing, with an access circuit, the one time programmable solid-state device.

30. The method of claim 29 wherein the programmable solid-state device is a solid-state imaging device.

31. The method of claim 30 further includes identifying a defective pixel within the solid-state imaging device.

32. The method of claim 29 wherein the driver circuit and access circuit are embedded in the die.

33. The method of claim 32 wherein the programmable solid-state device is an solid-state imaging device.

34. The method of claim 29 wherein writing further includes storing a code in the programmable memory unit.

35. The method of claim 34 wherein the code is a serial number.

36. The method of claim 34 wherein the code is a product identifier.

37. A method of data storage comprising:

identifying an address of a defective pixel in a photosensor having a plurality of pixels arranged in a two-dimensional array in a die within a programmable solid-state imaging device; and

storing the address in a programmable memory unit that is embedded in the die of the solid-state imaging device.

38. The method of claim 37 wherein identifying includes identifying a row and a column that corresponds to the defective pixel in the photosensor.

39. The method of claim 38 wherein storing includes permanently encoding the address of the defective pixel in the programmable memory unit.

40. The method of claim 39 wherein storing further includes permanently encoding the address into a row having a plurality of transistors in the programmable memory unit, where each transistor in the plurality of transistors has a gate.

41. The method of claim 40 wherein storing further includes breaking down the gate on each transistor in the plurality of transistors that corresponds to a logic 1 in the address.

42. The method of claim 41 further includes accessing the address stored in the programmable memory unit.

43. The method of claim 42 wherein accessing further includes detecting a leakage current flowing through the gate oxide of at least one of the transistors.

44. The method of claim 43 wherein accessing further includes amplifying the detected leakage current.

45. A one time programmable solid-state device comprising:

a programmable memory unit embedded in a die within the one time programmable solid-state device;

means for programming the programmable memory unit; and

means for enabling access to the programmable memory unit.

46. The one time programmable solid-state device of claim 45 wherein the programmable memory unit includes a number of memory cells with each memory cell of the number of memory cells having a gate.

47. The one time programmable solid-state device of claim 46 wherein the memory cells are arranged in a two-dimensional array having a number of rows of memory cells and a number of columns of memory cells.

48. The one time programmable solid-state device of claim 47 wherein the number of rows of memory cells is equal to a predetermined number, and the number columns of memory cells is equal to the predetermined number.

49. The one time programmable solid-state device of claim 46 wherein the solid-state device is an application specific integrated circuit (ASIC) having at least one predetermined configuration value in the programmable memory unit.

50. The one time programmable solid-state device of claim 45 wherein the programming means and access enabling means are embedded in the die.

51. A one time programmable solid-state device comprising:

means for writing to a programmable memory unit embedded in a die within the programmable solid-state device and

means for accessing the one time programmable solid-state device.

52. The one time programmable solid-state device of claim 51 wherein the programmable solid-state device is a solid-state imaging device.

53. The one time programmable solid-state device of claim 51 wherein the writing means further includes means for storing a code in the programmable memory unit.

54. The one time programmable solid-state device of claim 53 wherein the code is a serial number.

55. The one time programmable solid-state device of claim 53 wherein the code is a product identifier.

56. The one time programmable solid-state device of claim 51 wherein the writing means and accessing means are embedded in the die.

57. A one time programmable solid-state device comprising:

means for identifying an address of a defective pixel in a photosensor having a plurality of pixels arranged in a two-dimensional array in a die within a programmable solid-state imaging device; and

means for storing the address in a programmable memory unit that is embedded in the die of the solid-state imaging device.

58. The one time programmable solid-state device of claim 57 wherein the identifying means includes means for identifying a row and a column that corresponds to the defective pixel in the photosensor.

59. The one time programmable solid-state device of claim 58 wherein the storing means includes means for permanently encoding the address of the defective pixel in the programmable memory unit.